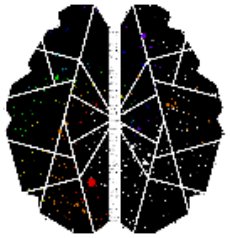


inNuCE LAB
Neuromorphic Computing
& Engineering LAB

Politecnico
di Torino

EDA

Neuromorphic Computing for AIoT Applications

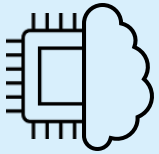
Neuromorphic Hardware and Algorithms Workshop
University of Sussex, 11th June 2026

Andrea Pignata
andrea_pignata@polito.it

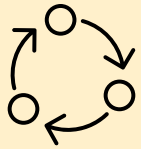
A brief presentation

- **PhD Student** in Computer and Control Engineering at Politecnico di Torino, Italy
- **Master Degree** in Computer Engineering, Embedded Systems track
- Part of the **inNuCE Laboratory**, the EDA Group branch involved in Neuromorphic Computing
- Currently **collaborating** with TU Dresden on SpiNNaker2
- **My goal**: development of tools and frameworks to ease deployment of Neuromorphic AIoT applications.

Outline

1 

WHY AIOT AND NEUROMORPHIC COMPUTING?
Advantages and drawbacks

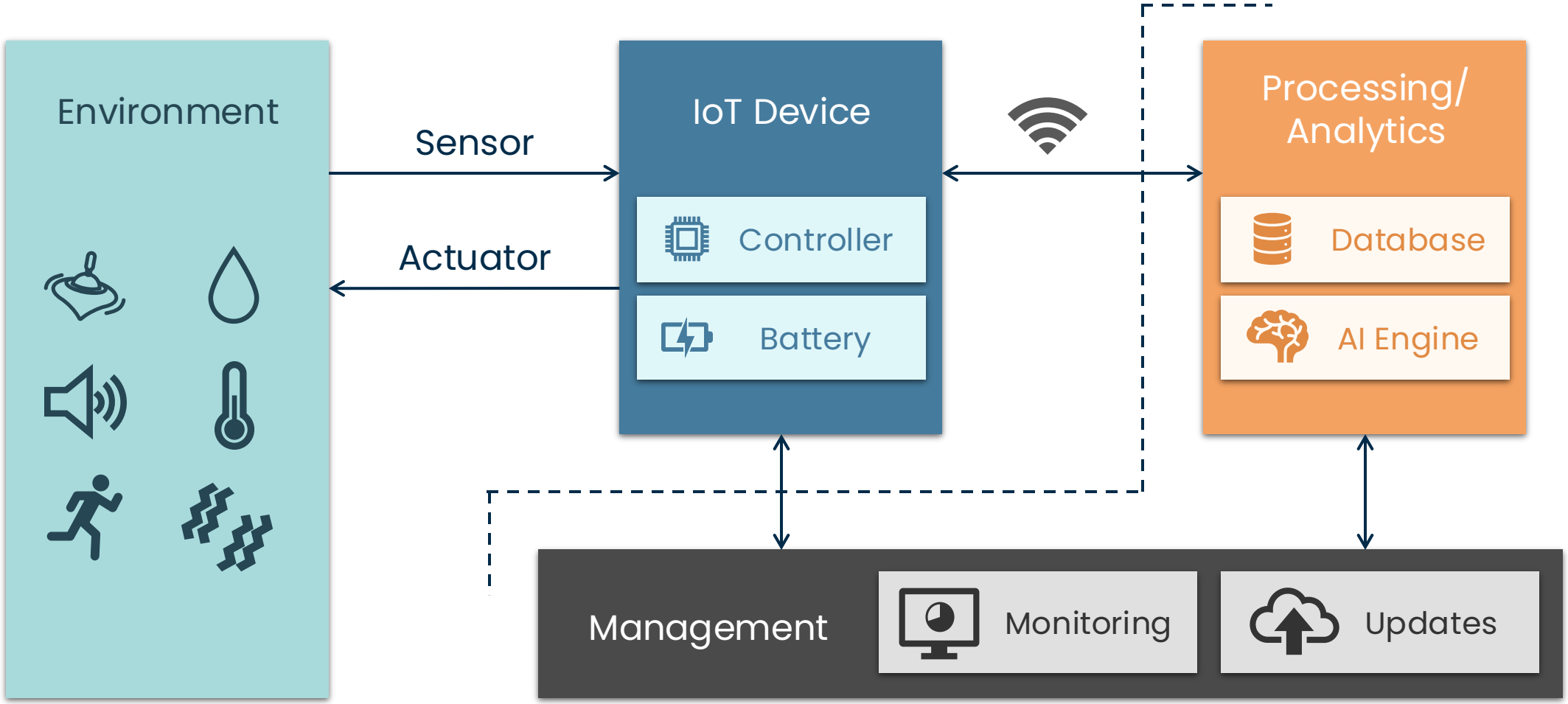
2 

ENABLING AIOT ON NEUROMORPHIC HARDWARE
The inNuCE Prototyping Platform and the NMLOps procedure

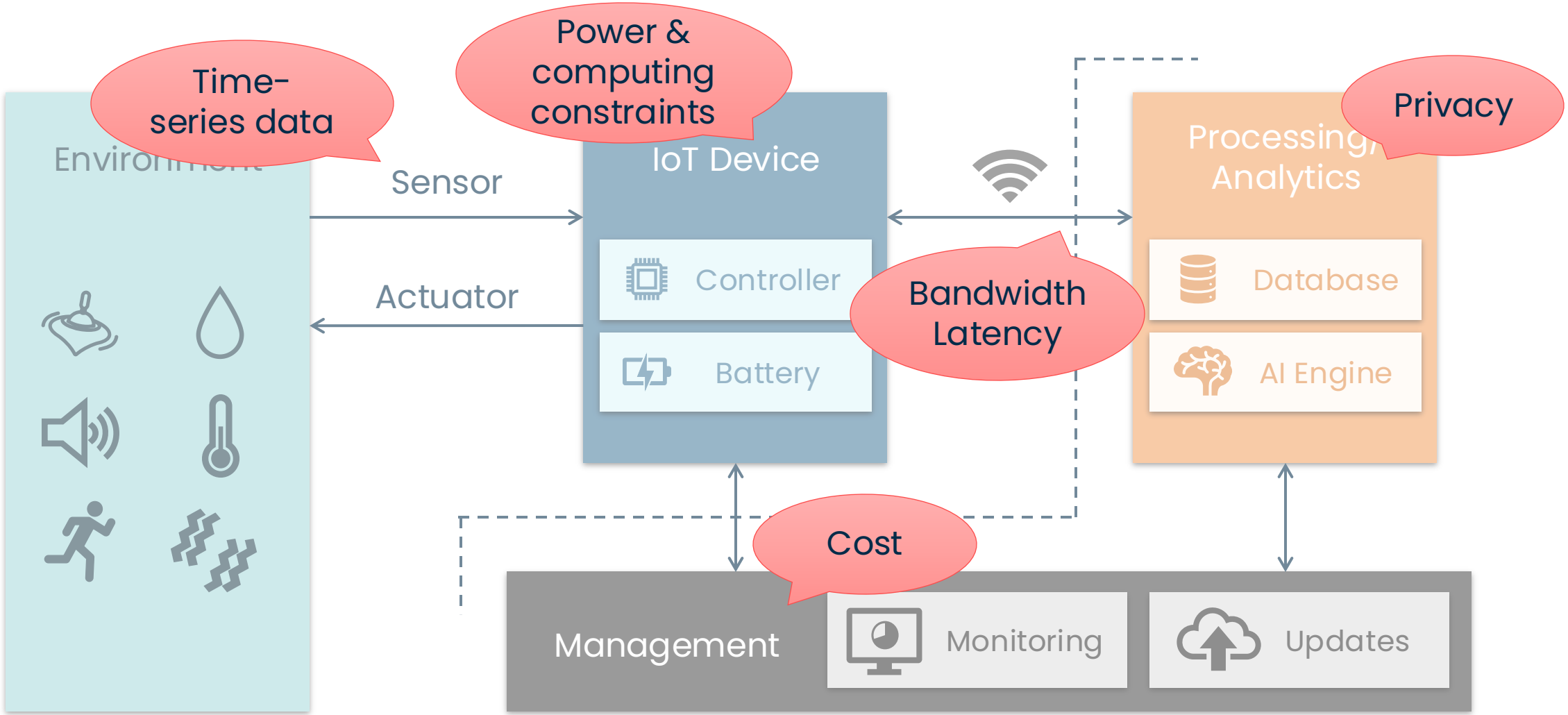
3 

EXAMPLES OF NEUROMORPHIC AIOT APPLICATIONS
Human Activity Recognition, Braille Letters Reading, Localization

An overview on AIoT



An overview on AIoT



An overview on Neuromorphic Hardware

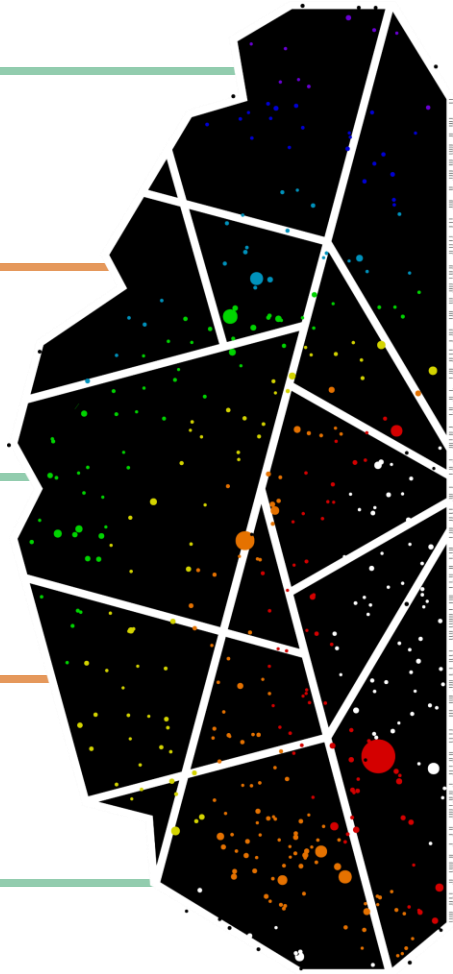
Support for Spiking Neural Networks
Biologically inspired, highly scalable

On-chip Inference
allowing edge AI in IoT

Spike-based communication event-driven behavior
Low power consumption

Online learning support
with on-chip, inference-time strategies

Highly coupled Processing and Memory
Efficient Hardware Design



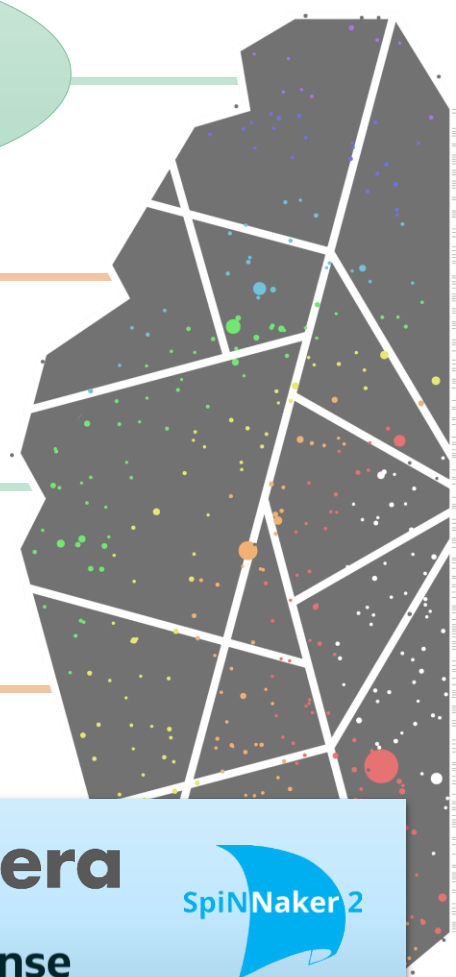
An overview on Neuromorphic Hardware

Support for Spiking Neural Networks
Biologically inspired, scalable

Time is modeled
Highly scalable

No Privacy & connectivity problems

On-chip Inference
allowing edge AI in IoT



Spike-based communication event-driven behavior
Low power consumption

Low power

No need for further infrastructures

Efficient computation

Online learning support
with on-chip, inference-time strategies

Highly coupled Processing and Memory
Efficient Hardware Design

brainchip
innatera
SpiNNaker 2
Noneuronova
SynSense

Challenges in Neuromorphic Hardware

Cost and Availability

- Few vendors
- Low availability
- Prices range ~200$ - 1000$

ANN: STM32 Devkits: 50$

Limited support

Limited support for neuron models and connectivity on HW

ANN: CPU/GPU are General Purpose units

Limited inter-operability

Absence of a common, standard language

ANN: ONNX/TF standards

Adoption of Neuromorphic Technologies *currently*

- ❌ Is expensive
- ❌ Requires high engineering efforts
- ❌ Limits reusability
- ❌ is hard to maintain

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Adoption of Neuromorphic Technologies *currently*

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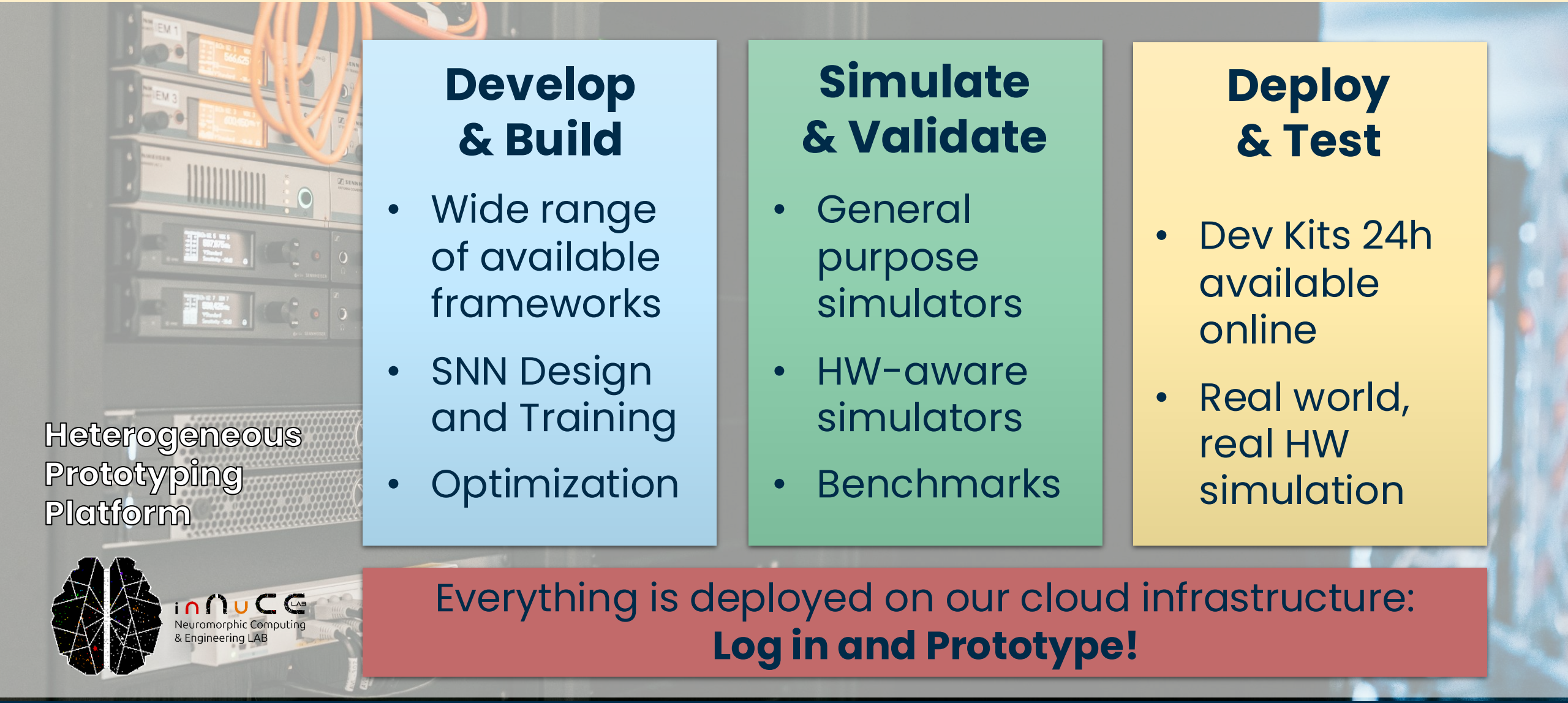
Opportunities:

Definition of a **standardized procedure** for Neuromorphic AIoT development

Development of a **cloud-based, shared** prototyping infrastructure

The inNuCE Research Infrastructure



Heterogeneous Prototyping Platform

Develop & Build

- Wide range of available frameworks
- SNN Design and Training
- Optimization

Simulate & Validate

- General purpose simulators
- HW-aware simulators
- Benchmarks

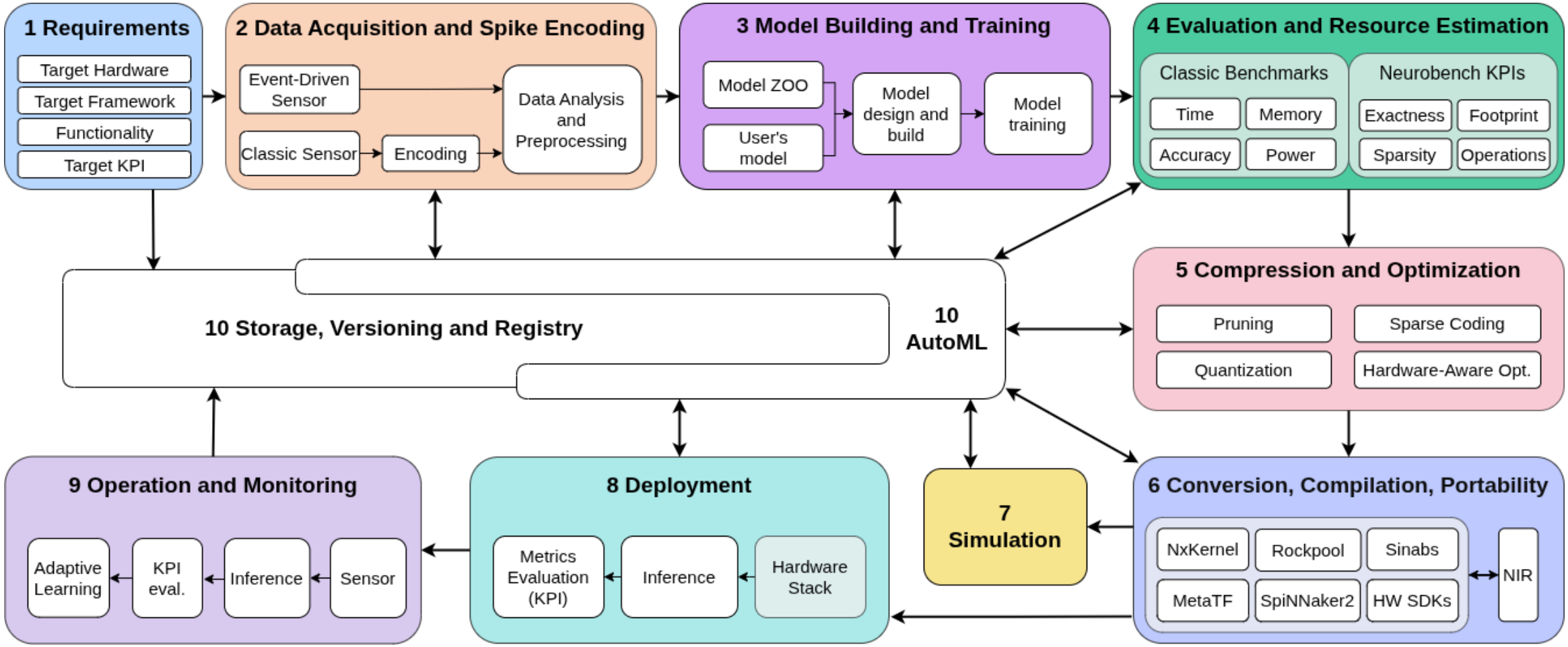
Deploy & Test

- Dev Kits 24h available online
- Real world, real HW simulation

inNuCE LAB
Neuromorphic Computing & Engineering LAB

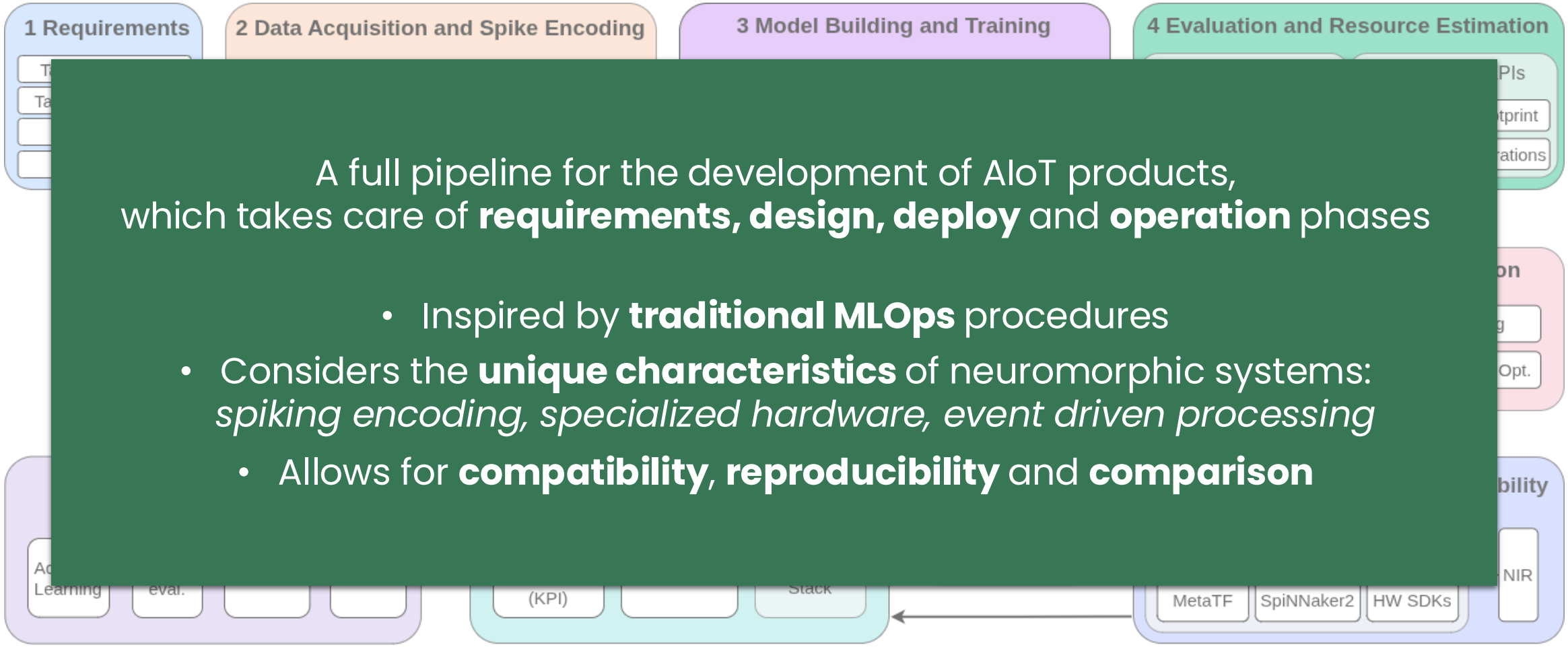
Everything is deployed on our cloud infrastructure:
Log in and Prototype!

The NMLOps Procedure



Urgese et et al. - IEEE Journal on IoT 2026

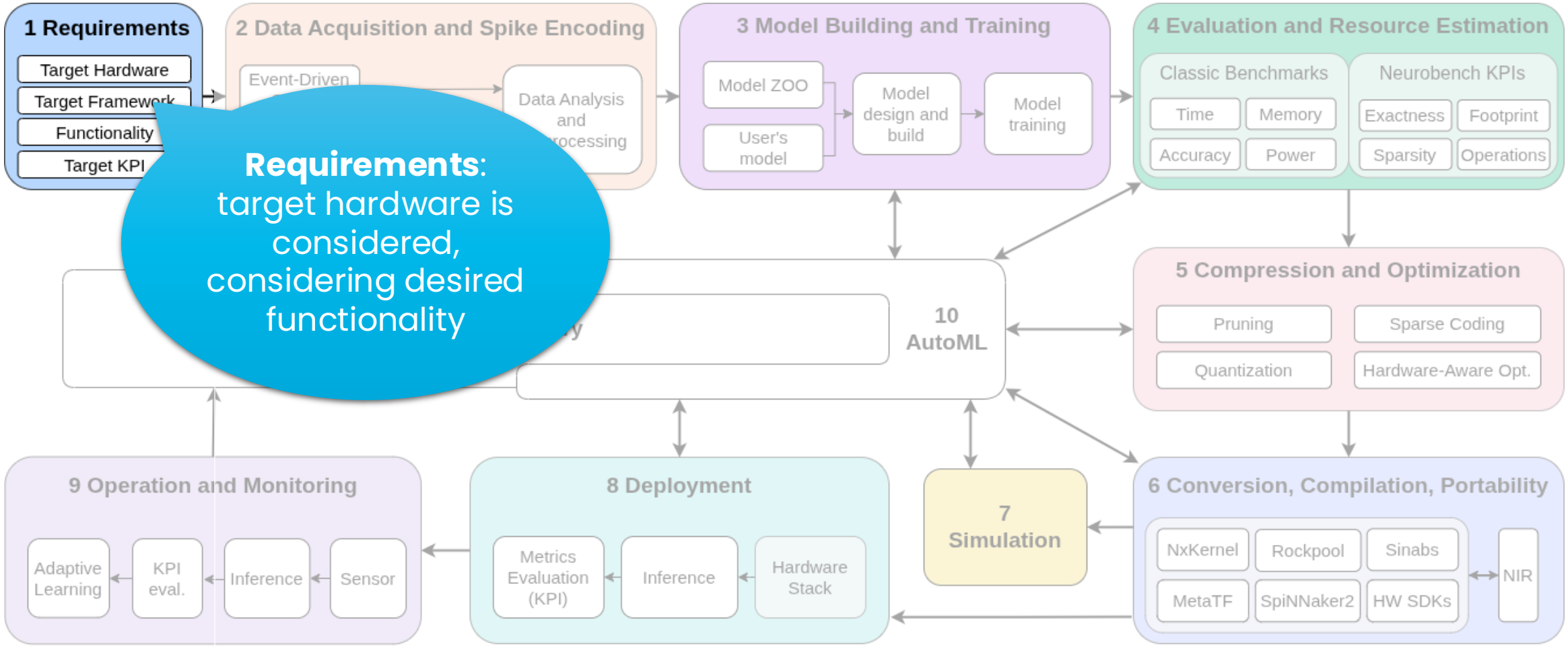
The NMLOps Procedure



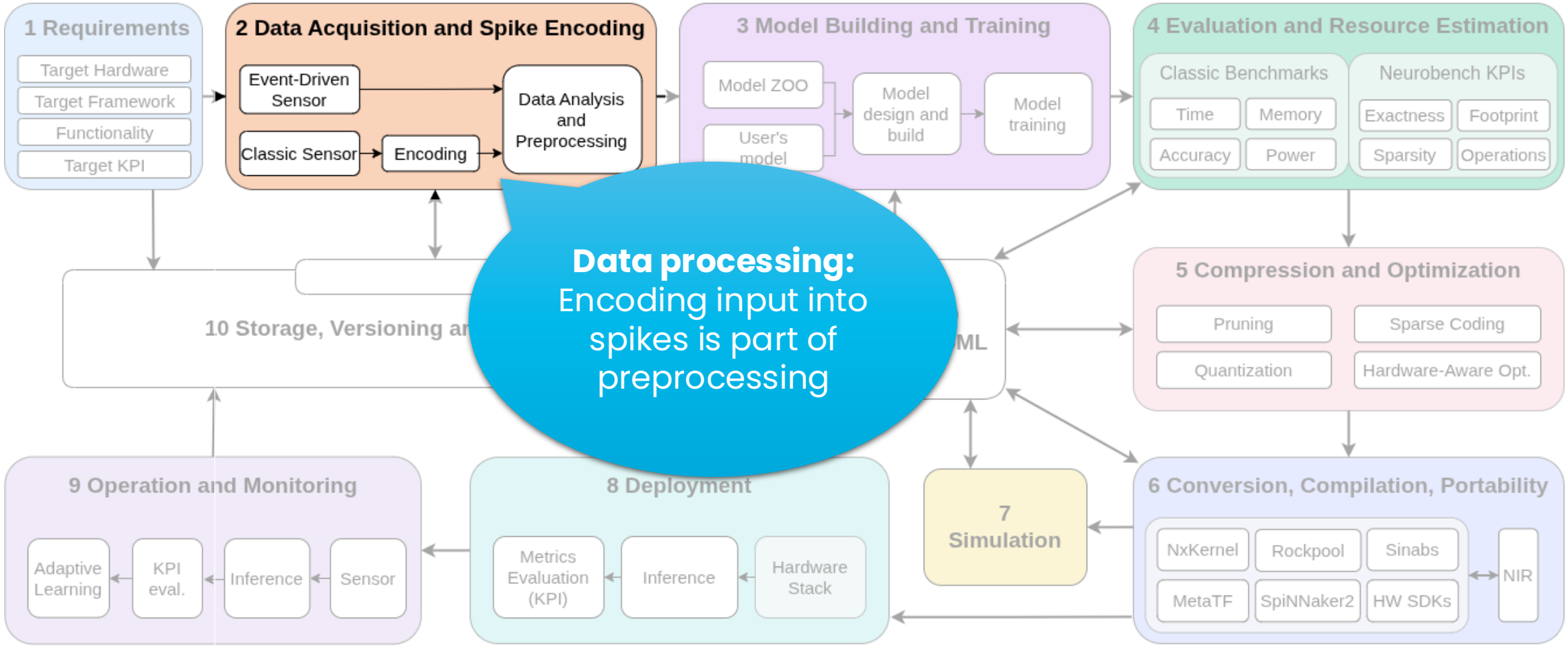
A full pipeline for the development of AIoT products,
which takes care of **requirements, design, deploy** and **operation** phases

- Inspired by **traditional MLOps** procedures
- Considers the **unique characteristics** of neuromorphic systems:
  spiking encoding, specialized hardware, event driven processing
- Allows for **compatibility**, **reproducibility** and **comparison**

The NMLOps Procedure



The NMLOps Procedure



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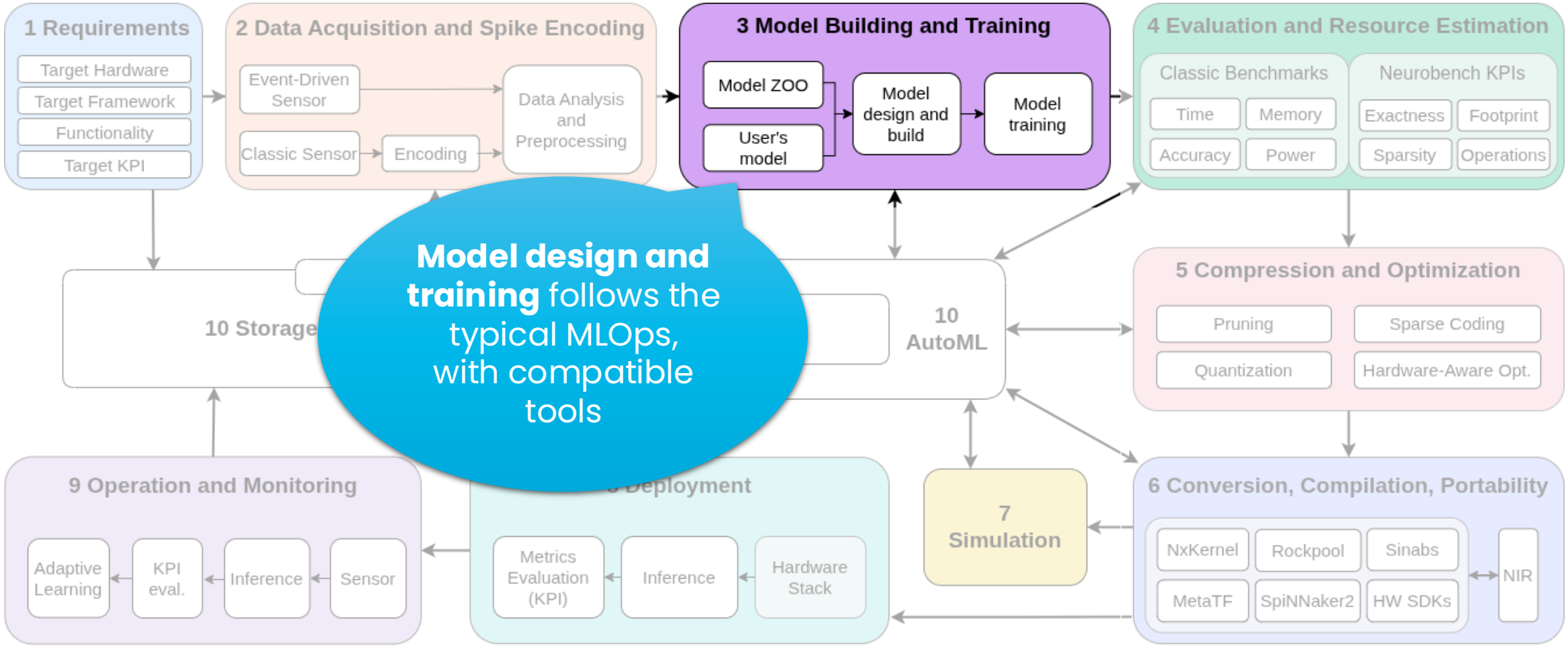

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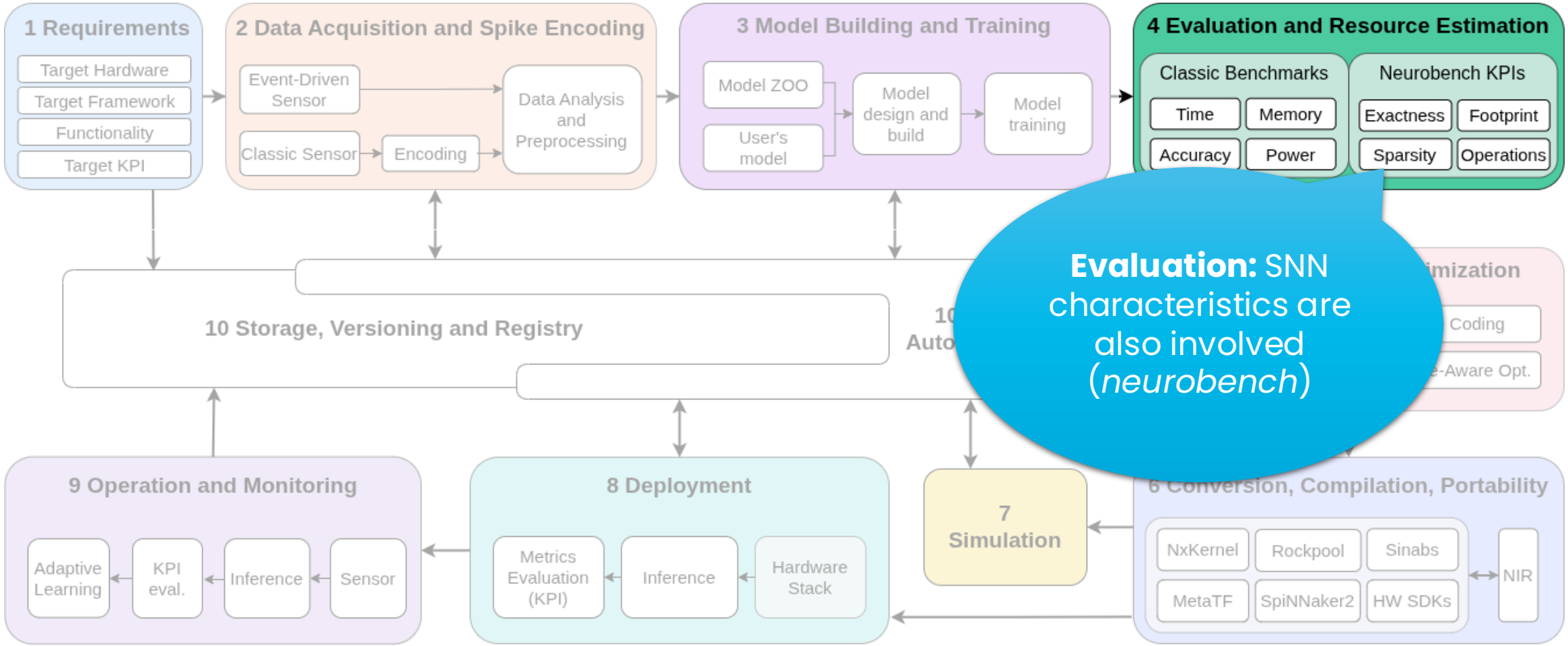
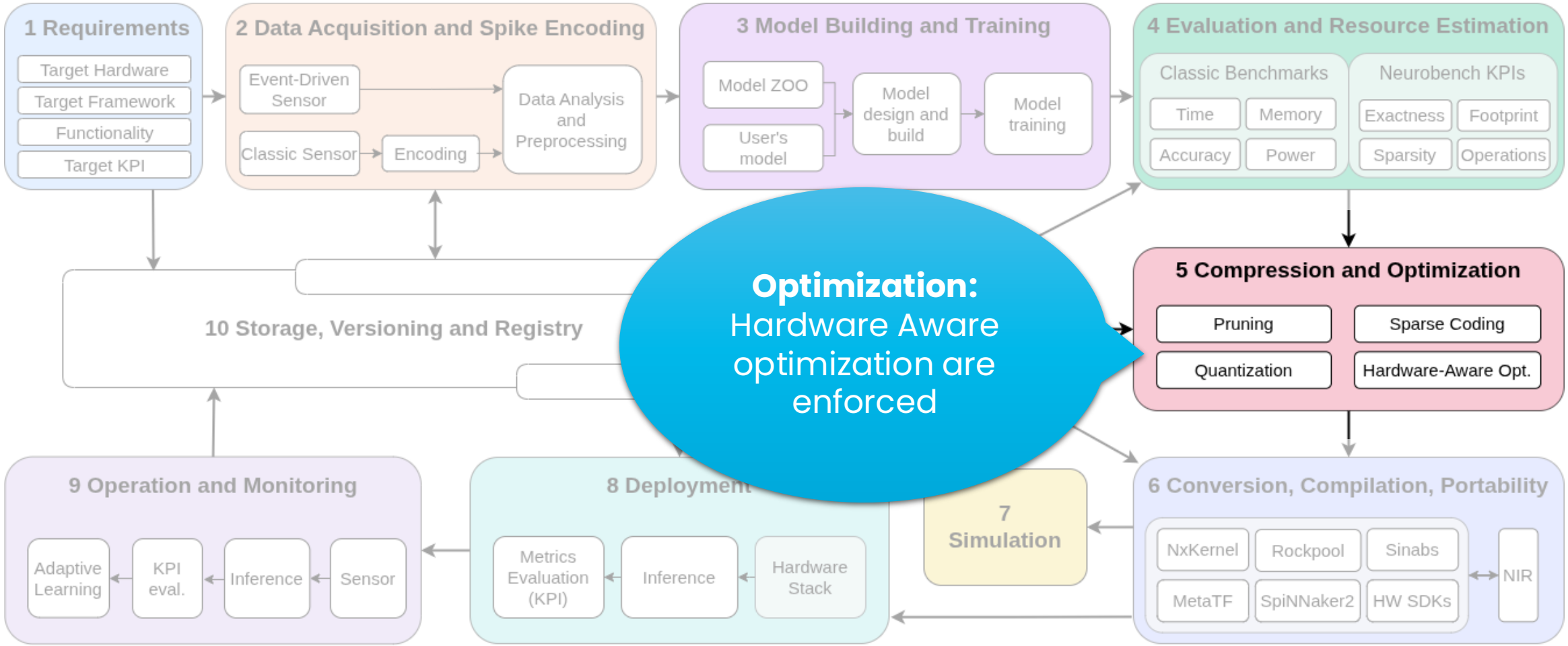


The NMLOps Procedure



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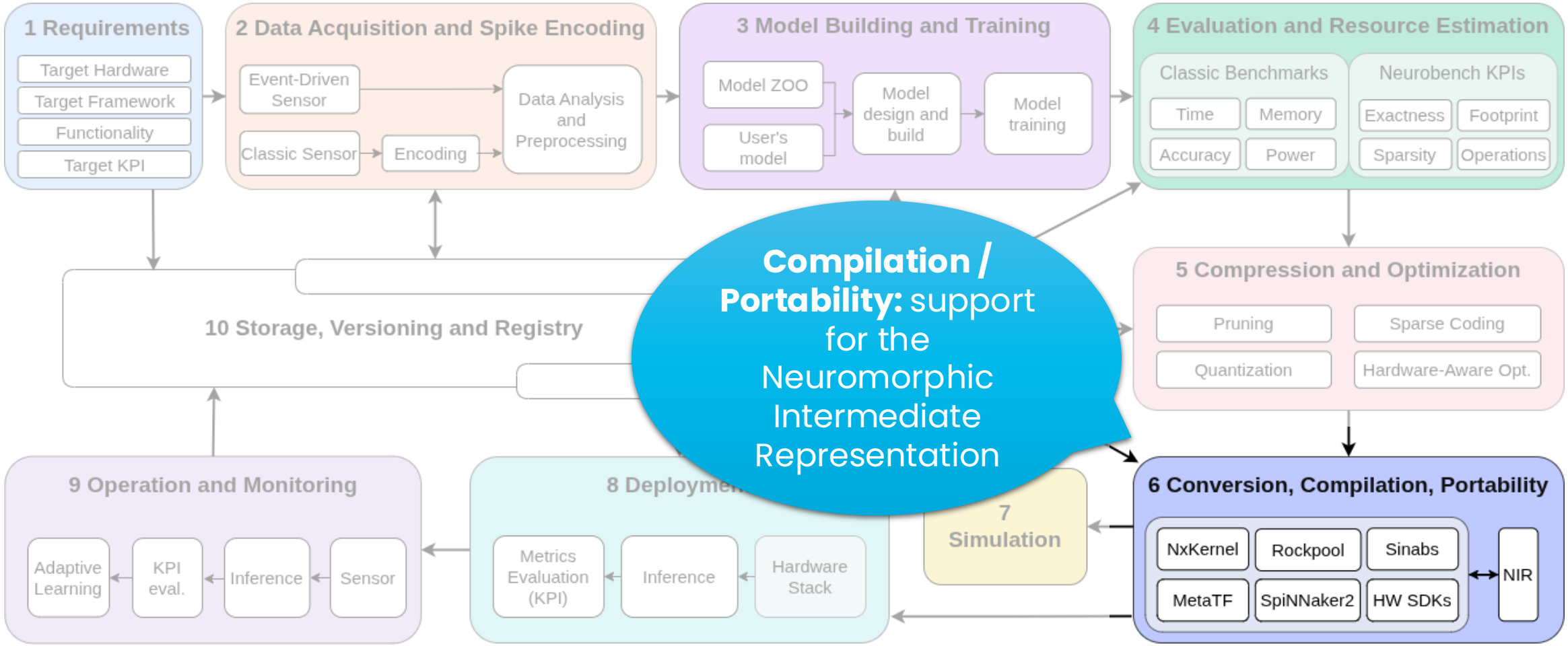
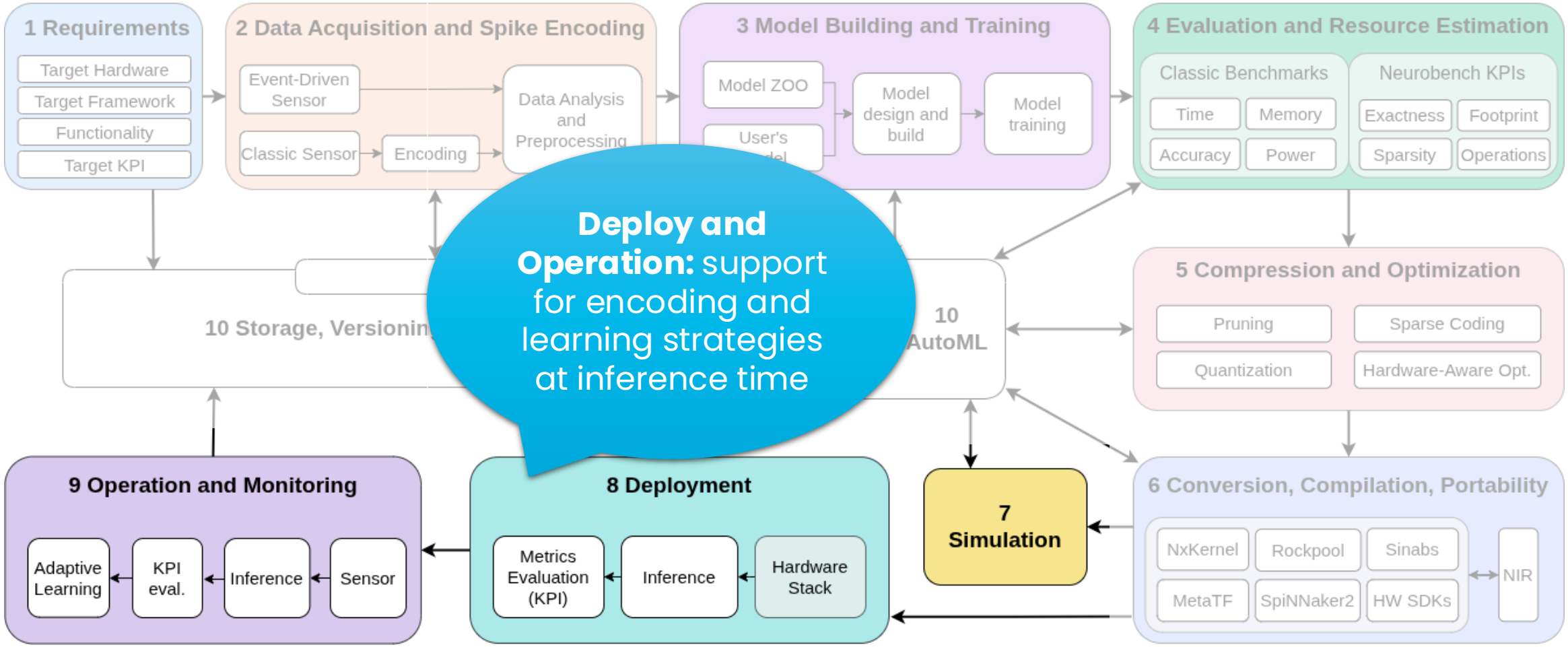
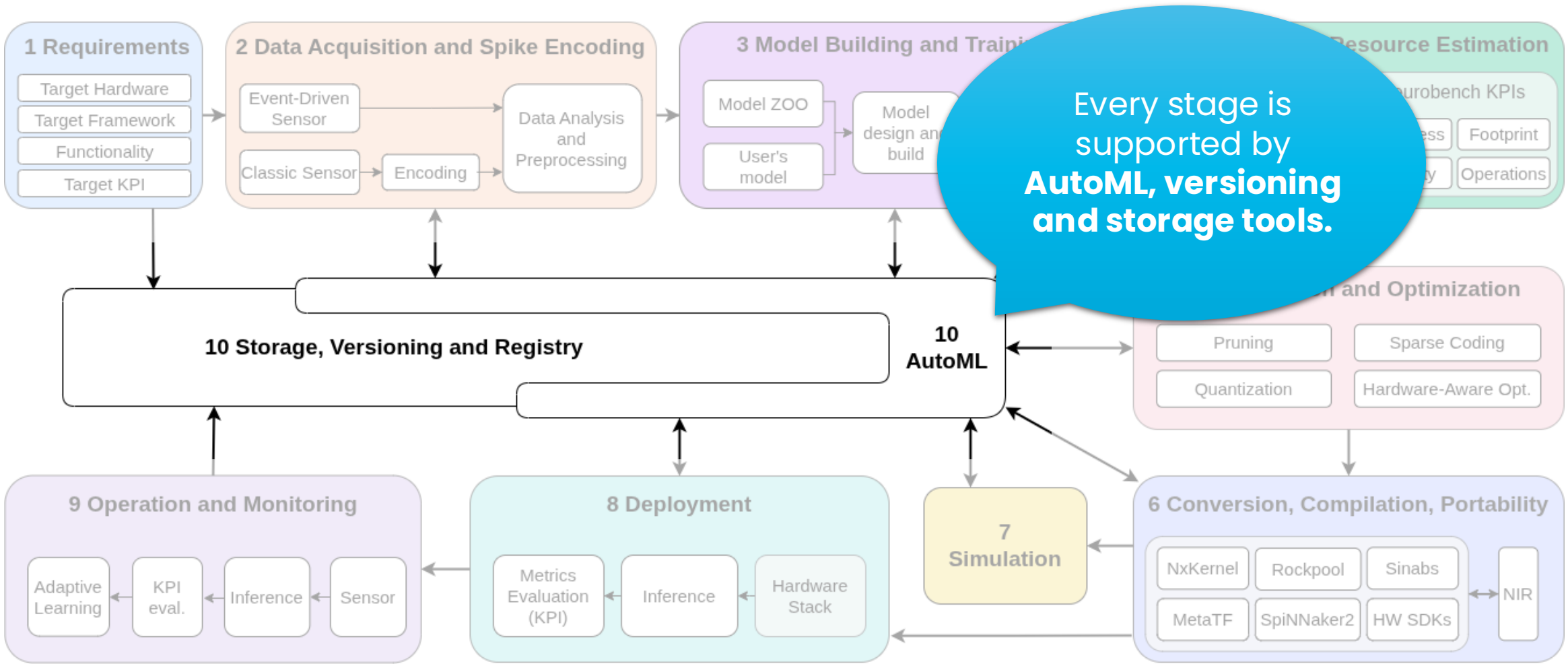


The NMLOps Procedure

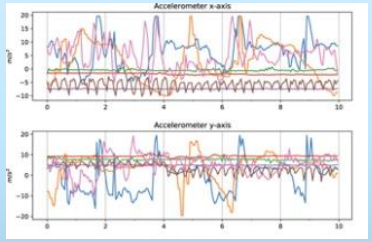


The NMLOps Procedure



Human Activity Recognition

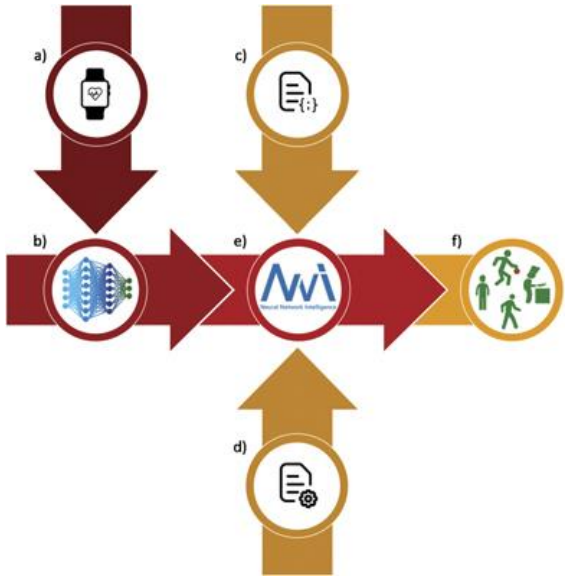
🚶 **DATA:**
IMU sensor (accelerometer & gyroscope)



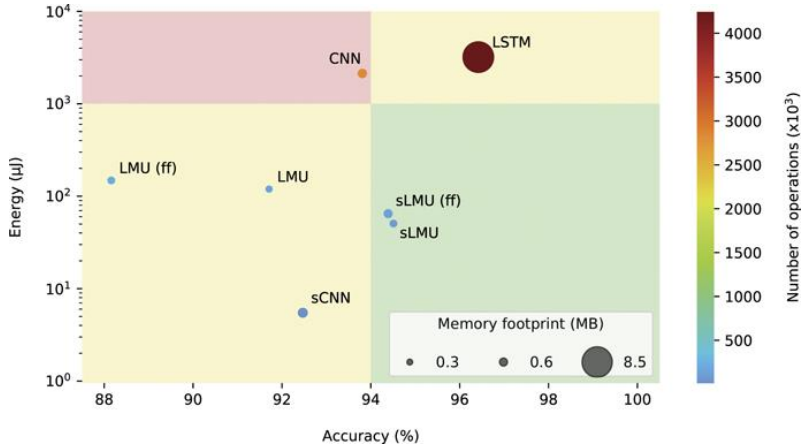
📈 **ENCODING:** Spike-rate

🧠 **MODEL(s):**
Spiking: sCNN, sLMU
Traditional: CNN, LMU

💻 **HW and SW:**
Nengo, snnTorch, Lava
CPU/GPU, Loihi2



Pipeline involves AutoML tools and multiple optimization iterations.



Versioning and reproducibility allowed comparison btw models

Fra et al. IOP-NCE 2022
Yik et al. Arxiv 20224 (Nature)
Fra et al. ICANN 2024

Rock Scissors Paper

🚶 **DATA:**
DVS (Dynamic Vision Sensor)

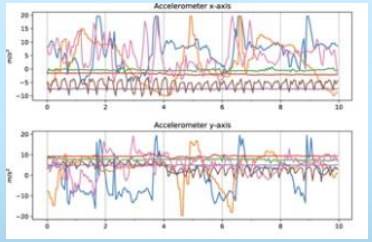
📈 **ENCODING: not needed!**

🧠 **MODEL(s):**
Spiking CNN

💻 **HW and SW:**
snnTorch, Sinabs
Synsense Speck, Brainchip Akida

End-to-End Dead Reckoning

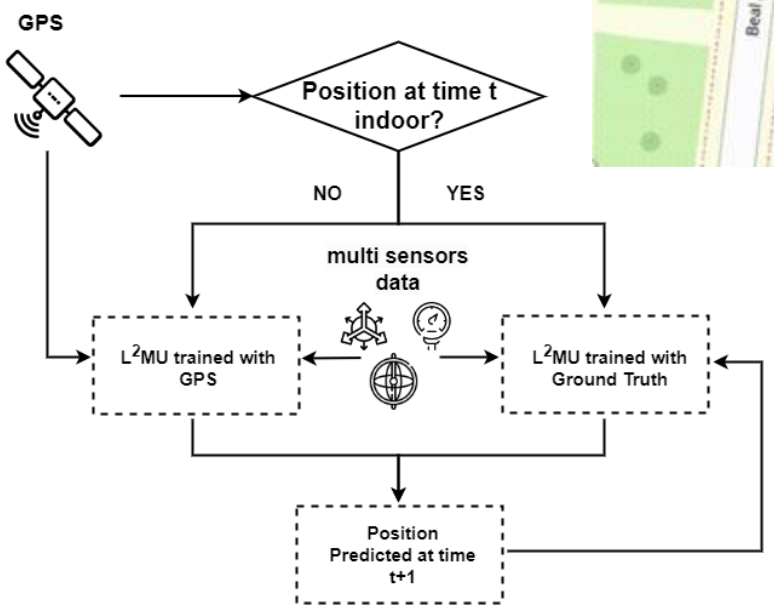
🚶 **DATA:**
GPS + IMU (accelerometer & gyroscope)



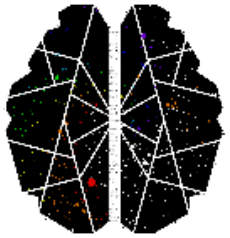
📈 **ENCODING:** LIF-Based

🧠 **MODEL(s):**
Spiking Legendre Memory Unit (L^2MU)

💻 **HW and SW:**
snnTorch, GPU



S. Tilocca et al. – NICE 2025



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